TAHA IQBAL

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EDUCATION

University of Saskatchewan **Sept. 2024 – Present**

Bachelor of Science in Electrical Engineering – 3rd Year *Saskatoon, SK*

- **Related Courses**: Logic Design Using FPGAS, Microprocessor Embedded Systems, Embedded Machine Learning

PROJECTS

32-bit RISC-V CPU | SystemVerilog, Icarus Verilog, GTKWave, Git/GitHub

- Designed and implemented a **32-bit single-cycle RISC-V CPU** in SystemVerilog, integrating a custom ALU, 32x32-bit register file, program counter, instruction decoder, control unit, and memory modules
- Developed **self-checking SystemVerilog testbenches** for each RTL module, verifying reset behavior, register semantics, dual-port reads, ALU operations, and control logic through automated pass/fail testing
- Implemented **RV32I R-type and ADDI instruction execution**, including opcode/funct decoding, immediate sign-extension, register write-back, and ALU control
- Verified the integrated CPU by **hand-encoding and executing RISC-V machine instructions** in Icarus Verilog and debugging signal behavior with GTKWave

IoT Mailbox Simulator | Python, Multithreading, Event-Driven Programming, Git

- Designed a **Python-based mailbox** using **callback-driven sensor** monitoring and multithreading to model mailbox door open and close events from LED light-level signals
- Built a command-line interface tool that monitors system activity while running asynchronously, supporting safe start/stop operations, with a modular design and Git workflows for maintainability and version control

TV Remote Controlled Rover |C, Embedded Systems, IR Control

- Programmed a rover to navigate a maze using **infrared commands from a TV remote**
- Developed embedded **control logic for navigation and obstacle handling** using sensor inputs

WORK EXPERIENCE

Software Developer **Jan. 2026 – May. 2026**

MiMinions *Saskatoon, SK*

- Collaborated within a team of 4 to build a scalable, modular platform for orchestrating AI agents in Python, contributing through a structured project placement
- Re-architected the workflow tracing system by introducing WorkflowTrace, a flat ordered sequence that replaced a nested trace structure, simplifying traversal and reducing complexity across the execution pipeline
- Refactored core modules with incremental commits to improve system modularity and maintainability
- Applied Test-Driven Development with pytest, extending to validate trace ordering and prevent regressions

Cybersecurity Intern **Oct. 2025 – Jan. 2026**

The Clean Divorce *Saskatoon, SK*

- Performed **security risk assessments** on customer management platform to find vulnerabilities in data storage
- Researched **7+** platforms and **assessed security** based on encryption, document storage, and data protection
- Evaluated layered protection strategies, and **recommended practices** to stakeholders on strengthening security

SKILLS

- **Languages:** SystemVerilog/Verilog, Python, C, Java, JavaScript, MATLAB
- **Embedded:** Arduino, ARM Cortex-M4F, GPIO, Register-Level Programming
- **Digital Design:** RISC-V (RV32I),RTL Design, FPGA Design, Digital Logic, State Machines
- **Tools:** Intel Quartus, Icarus Verilog, GTKWave, Code Composer Studio, LTspice, Git, Linux, Windows